Kunden Service
Bischoff Analysentechnik GmbH

Optichrom Advance
Technische Information

Mini-Manual for ACB2
Analyzer Controller Board
2000212

1. Introduction

The 2000212-001 (ACB2) is an enhanced version of the 2000120-001 controller board (ACB) for use in Advance analyzers. It is intended to replace the 2000120-001 in all applications. With a mounting adapter kit, the new board can be exchanged for the older model; the program loaded; and the application run with no changes to the application program.

2. Important Part Numbers

2000212-001 - ACB2

Assembled and tested controller board

2000400-006C - ACB2 Mounting Bracket Kit

Mounting bracket to replace ACB with ACB2 in a door. Includes bracket and all required screws, washers, etc.

2000400-006 - Door with ACB2

Assembled Door with ACB2 installed.

2000243-001 - Field Programming Kit

Complete kit to allow upgrade of the ACB2 firmware in the field. Includes field programming disk and cables.

2000214-001 - Field Programming Disk

Disk containing upgrade firmware for field programming kit.

Part Number Translation Table		
With 2000120	**With 2000212**	**DESCRIPTION**
2000400-005	2000400-006	DOOR ASSY, W/STD CMPNTS, INTERNATIONAL
2000448-004	2000448-006	BASE CHROMATOGRAPH PLUS THERM DET.
2000448-005	2000448-007	BASE CHROMATOGRAPH PLUS TCD W/O OVEN
2000449-003	2000449-004	BASE CHROMATOGRAPH PLUS DUAL THERM DET.
2000450-006	2000450-009	BASE CHROMATOGRAPH PLUS FID
2000450-007	2000450-008	BASE CHROMATOGRAPH PLUS FID, W/O OVEN
2000495-002	2000495-003	ADVANCE ELECTRONIC CONTROLLER MODEL EC
2000645-002	2000645-004	CHROMATOGRAPH, TCD, W/VALVES, REGULATORS
2000645-003	2000645-005	CHROMATOGRAPH, TCD, W/VALVES, REGULATORS, CRATED
2000646-001	2000646-003	CHROMATOGRAPH, FID, W/VALVES, REGULATORS
2000646-002	2000646-004	CHROMATOGRAPH, FID, W/VALVES, REGULATORS, CRATED
2000647-002	2000647-003	BASE CHROMATOGRAPH PLUS FID / TCD
2013700-002	2013700-003	PROGRAMMED TEMPERATURE GAS CHROMATOGRAPH

3. ACB2 (2000212-001) features

3.1 Functionally compatible in existing Advance analyzers

3.2 More memory:

256K Flash memory for firmware.

1 Mbyte of RAM for everything else, see the table below.

Memory comparison table

Use	ACB 1		ACB 2	
	Size	Points	Size	Points/Records
FLASH	128K	-------	256K	-------
System RAM	32K	-------	96K	-------
Data base RAM	32K-64K	128 - 256 blocks	64 b	256 blocks max
Data Table RAM	-------	-------	384 bytes - 863.5K	max 65,535 / stream max 73,684 total
Chrom Table RAM	32K - 64K	max 21,845	15 bytes - 863K	max 65,535 / record max 294,613 total
Total RAM	128K		1 Meg	

NOTES:

- With ACB 1, Data Base Tables and Chrom Table share 32K of common ram.
- With ACB 2, Chrom table and Data Table share 863.5K of common ram.
- Chrom table must have at least 1 point for each of the 5 records.
- Chrom table uses 3 bytes per data point.
- The data table has 32 “streams”. The data table must have at least 1 record defined for each of the 32 streams.
- The data table uses 12 bytes per record.
- The data base uses 256 bytes per block. The final block can only be used by ACB 2 for chrom and data table.

3.3 Firmware field upgrade capability.

Using the field upgrade kit and a Personal Computer, the Advance Firmware in the FLASH memory on ACB2 can be upgraded on-site.

3.4 Separation of Chromatogram space and Program space.

Programs and Chrom records no longer use overlapping space. All 64k of program space is available for program regardless of Chrom records being kept. Chrom records can now be up to 65,535 points each.

3.5 Data Tables.

Another method of saving program memory is to use the new Data Tables for information storage instead of Result Tables, Buffer Tables, or Factor Tables. The data tables are stored outside program space. See the section on Data Tables for additional details.

3.6 Enhanced data acquisition:

Sample rate of up to 100 points per second on 4 detectors in fast chromatography applications.

16 bit data precision with 22 bits of range.

The ITC can now be used as a third spare input. (See "Using the ITC as a Spare Input")

Improved noise levels on detector and spare inputs.

3.7 Enhanced processing power:

68332 microprocessor running at 16.8 Mhz

Program execution speed increase of about 5 times.

Increased speed for calculation intensive applications of about 7 times.

3.8 Enhanced design for EMC.

Filtering has been added to all I/O and power lines to reduce interference from RF signals, and to reduce the interference being emitted by the ACB2. Multilayer design techniques have produced a board that is inherently less noisy and less susceptible to noise pickup.

3.9 "Normal", "Warning", and "Fault" lights for Data Hiway.

A green light indicates Hiway data transmit / receive in progress, a yellow light indicates a retry in progress, and a red light indicates a fault has occurred on one of the channels. Faults are: invalid loop number, duplicate loop number, invalid unit number, and duplicate unit number.

3.10 Uses long-life lithium battery instead of rechargeable NiCad.

The lifetime of this battery is expected to exceed 10 years, and is more environmentally sound.

3.11 Additional serial communications ports

These will be used in projects such as FTIR, and interfacing with continuous analyzers.

3.12 Firmware Changes:

Primarily, firmware changes were made to accommodate the hardware changes described above. In addition, all changes through version 3.8 of the 2000120 have been included, and a number of nuisance-behaviors have been corrected:

Duplicate analyzer no longer removes data base. Changes CTRL(12) to zero instead.

Trying to load a database from a cartridge that contains a chrom record no longer zeroes the Database.

Pressing a key during the cartridge load no longer resets the analyzer.

An analyzer with no tables now comes up with a "minimum" data base. This gives limited control so that some operations can be performed before loading a data base. Viewing loop and unit numbers, and setting the analyzer number for example.

Chart recorder maximum zero value has been increased from 1024 to 2048 to help with the display of reverse peaks.

etc.

4. ACB Functional Block Descriptions

4.1 Microprocessor:

The microprocessor executes firmware stored in the Flash memory, and performs the functions described in the user program. It is the source of timing and control for all activity in the EC. The watchdog timer circuit is internal to the Microprocessor and will reset the ACB if code execution strays from its prescribed path. The real-time interrupt which is used to control user event timing is generated by a counter internal to the Microprocessor. The microprocessor system clock is generated internal to the microprocessor using a Phase-locked loop circuit. Both of these clock circuits are based on an external oscillator input. Interrupts from the calendar clock and Data Hiway circuitry are also prioritized and processed by the Microprocessor.

4.2 Real-time Clock:

The Real-time clock is a very accurate oscillator with two square-wave outputs. One output is used by an internal counter in the Microprocessor to generate interrupts for Data acquisition and other events that must be timed very precisely. The other output is used in conjunction with a VCO which is internal to the Microprocessor to generate the Microprocessor's system clock.

4.3 Memory:

The Flash memory contains the firmware that controls program execution. The Flash memory can be reprogrammed without being removed from the PC board.

RAM contains the user program, system parameters, scratch pad memory, and collected data such as data tables and chromatograms. The RAM has battery back-up so that all information is maintained when system power is removed.

4.4 Battery Backup:

Backup power for the Calendar Clock and RAM is supplied by a lithium battery when the system power is removed. The battery will maintain information stored in RAM and keep the calendar clock running for more than 20 years at room temperature and 5 years at elevated temperatures. A jumper on the board allows the battery to be disconnected from the RAM and Calendar Clock if the board is to be stored for an extended period during which keeping time and data is not important.

4.5 Power Monitor and Push-button Reset:

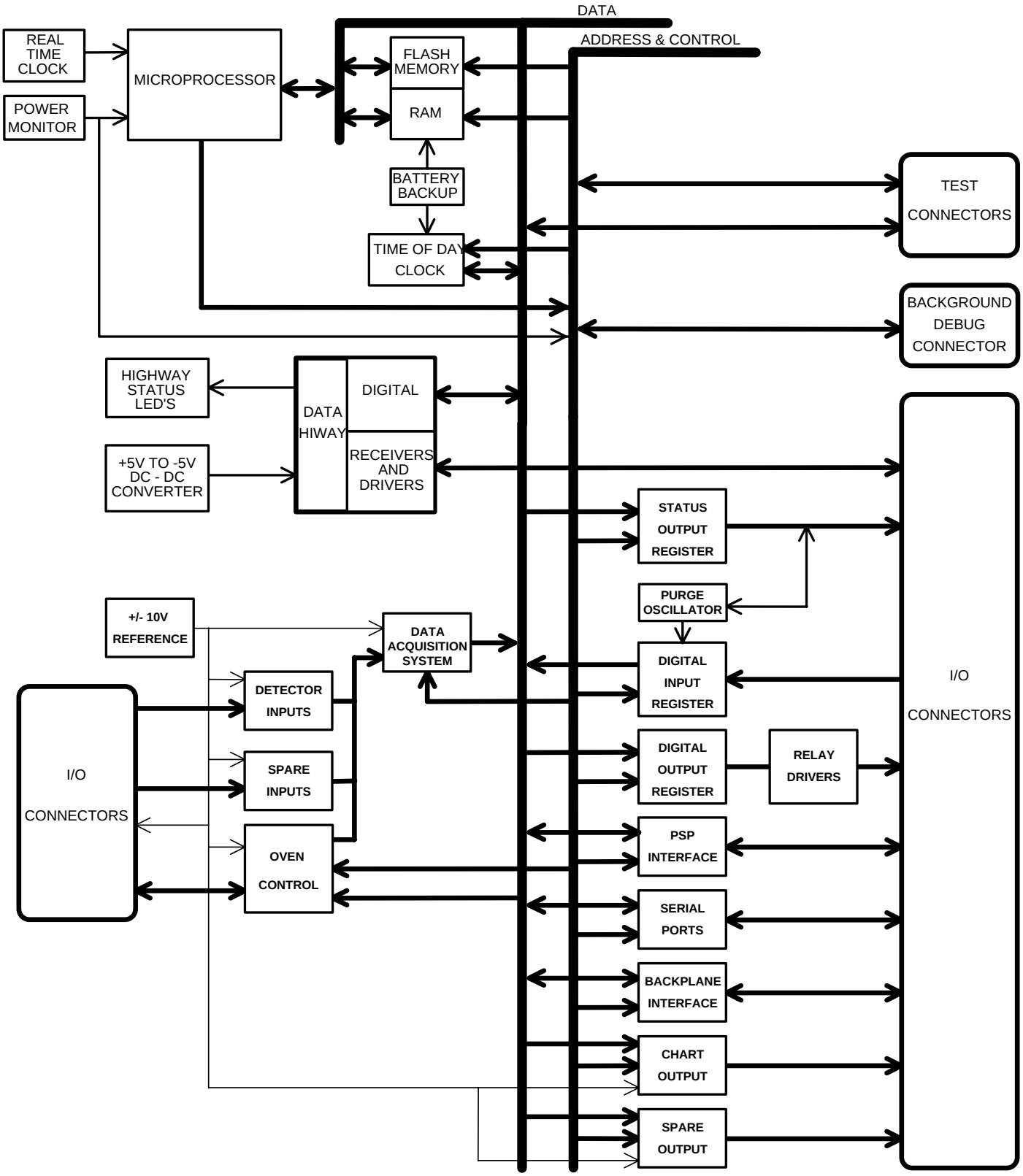
This circuit continuously monitors the 5V. power level. If the voltage drops too low, the Microprocessor reset will be held active to prevent program run-away or accidental writes of bad data to memory. At power-up, the microprocessor is held in reset until the 5V supply has reached acceptable limits, and for one additional second to insure proper initialization of hardware. The power monitor is also connected to a reset switch which can be used to manually force a system reset.

4.6 Time of Day Clock:

This clock keeps track of the date and the time of day to the nearest second. In system operation it provides an interrupt each second that is used to trigger certain types of events. Since the clock is supplied battery power when the normal power source is removed, time keeping is not interrupted by power outages.

4.7 DC-DC Converter:

A DC-DC converter is used to generate -5v from the +5v power supply. This supply is used to operate the differential drivers in the Data Hiway circuit that drive the cable.



ACB2 Block Diagram

4.8 Data Hiway Interface:

The Data Hiway circuitry allows communication between the ACB and any other AAI H&B unit that has Advance Data Hiway communication capability. The LOOP and UNIT switches are used to determine the Data Hiway address to which a unit will respond.

The Data transmission path is from the Microprocessor to a serial port through a Manchester Encoder, to the differential drivers that drive the carrier and data signals onto the cable. The receivers are connected to the same cable. They separate data from carrier and convert the signals from their transmission form to digital form. The data is then sent through a Manchester decoder to a serial port which is read by the Microprocessor.

The Data Hiway circuit has two channels to provide redundancy in the case of a channel failure. If a channel failure occurs, data will be routed through the other channel.

In order to prevent a single unit from taking control of the Hiway and never relinquishing control, there is a hardware fail-safe timer for each Hiway channel. The timer monitors how long its unit has been transmitting on the Hiway, and if it times out, the offending channel's driver is disabled and a red lockout-indicator is activated. The lockout remains in effect until a system reset occurs.

The Hiway circuit also contains timers that control contention timing, and indicators that show the state of activity. The green light shows normal activity. Yellow is a message retry. Red indicates Hiway failure.

4.9 Backplane Interface:

This is the interface to the I/O backplane in the GC. Most of the logic for this interface is contained in a Programmable Logic Device which directly drives the backplane from the ACB through connector J7. This interface converts the signals on the microprocessor bus to the correct timing and format to communicate with the boards that plug into the I/O backplane.

4.10 PSP Interface:

This interface allows the microprocessor to communicate with the Portable Service Panel through the intrinsic barrier board. It is a dual 8-bit parallel interface one port for control signals and one for data. These ports allow the microprocessor to communicate with the UARTS on the Intrinsic Barrier Board which in turn communicate with the PSP through the intrinsic barrier.

4.11 Debug Interface:

This interface consists of a 10 pin connector that provides control of the microprocessor. During firmware debug, it allows debug functions to be performed such as setting breakpoints and viewing memory and registers without attaching an emulator. It can also be used to reprogram the FLASH memories on the board.

4.12 Purge Oscillator:

This circuit oscillates at about 1 cycle per second. It is used to flash the Purge Alarm indicator (one of the status outputs, see below) when purge has been lost. This is an independent circuit, it will flash when there is a purge fault even if the microprocessor is not working properly.

4.13 Status Outputs:

These are high-current drive outputs used to indicate analyzer status, and to control the chart drive. With the exception of the Purge Alarm (see above), they are under direct microprocessor control. There are six outputs, Purge, Fault, Warning, Normal, External Alarm, and Chart Drive. The Purge, Normal, Warning, and Fault outputs drive the LED’s visible from the front of the analyzer. One more

output is intended to drive a relay coil for an external alarm, and the Chart Drive output is used to start and stop the drive motor on a chart recorder. The chart drive output has a jumper which allows selection of the polarity of the output. All the other outputs are active low open-collector.

4.14 Digital Outputs:

There are eight high-current drivers used to drive relays on the relay board which are used to control solenoid valves. There are switches on the door that determine the mode in which these outputs work. The switches allow on / off manual control and auto mode. In auto mode, the outputs are under control of the user program.

4.15 Digital Inputs:

There are eight digital inputs. Four are available on the termination board for local input. The wires for these inputs are not protected from static discharge or electromagnetic radiation, so should be used only for equipment that has contact closure outputs located within or adjacent to the analyzer. The other four inputs reflect the status of circuits on the ACB. One input indicates to the firmware that a Daughter board is attached at J8. The other inputs indicate purge alarm, overtemp shutdown, and heater relay on or off.

4.16 ±10V References:

These highly accurate and stable reference voltages are used by the analog circuits to perform control and measurement functions. They determine the basic accuracy and noise level of the entire analog system.

4.17 Data Acquisition System (DAS):

These circuits measure the analog signals from the spare channels, temperature input and detector inputs. When taking measurements, the DAS looks at each signal, and selects a gain from 1 to 128 that gives the largest output that is within the measurement limits of the A/D converter. The A/D converts the analog signal to a 16 bit two's compliment number. The DAS then saves that number along with the exponent (the gain) in a FIFO. The data is taken from the FIFO by the microprocessor and used to update the AI tables and detector tables in the analyzer. The 16 bit converter and gain of up to 128 gives the DAS a resolution of 16 bits and an effective range of 23 bits. The measurements can be repeated up to 100 times per second. This is controlled by the analyzer clock rate in the control table.

4.18 Differential Detector Input:

This circuit is intended for use with thermistor or filament detectors. It compares the output of a sensor in a reference stream to the output of a sensor in the stream following the column. The difference is amplified and the balance value subtracted. The signal is then filtered and sent to the DAS for measurement.

4.19 ITC Detector Input:

The Inter-column detector circuit is less complicated, and is not as sensitive as the differential detector. After the balance value is subtracted, the signal is filtered and sent to the DAS for measurement. This input can also be used as a third spare input. See "Using the ITC as a Spare Input".

4.20 Spare Inputs:

The analog signals connected to these inputs (connections are made on the ATB) are filtered and sent to the DAS for measurement.

4.21 Chart Output:

This output is -20 ma to +20 ma full scale driven by a 12 bit DAC. It is intended to drive a chart recorder. Most chart recorders are 1v full scale input indicating the need for a 50 ohm resistor across the terminals at the chart recorder.

4.22 Spare Output:

This is a 0 to 10V full scale output from a 12 bit DAC available at connector J11. The DAC is addressable as channel 23.

4.23 Oven Control:

These circuits perform three functions. The first is oven temperature control. The setpoint is calculated and set by the microprocessor from values in the tables. The setpoint is then compared to the value from the oven temperature sensor, and used by the control circuit to turn the heater relay on and off. The control circuit varies the length of the on and off intervals as needed to reach and maintain the setpoint temperature. The control circuit is designed to minimize the time required to reach the set temperature, and to hold the temperature at a highly stable value.

The second function is to limit oven temperature so that the T rating for a given application can be guaranteed. A separate sensor is used to monitor the temperature, and compare to the limit set by the T-limit resistor. When the limit is reached, the circuit disables the driver to the heater relay preventing further heating.

The third function is a safety override called over-temp shutdown. It is a completely independent circuit with its own sensor, power regulator, and heater relay. The relays for this circuit and the temperature control circuit are wired in series so that both must be activated to provide power to the heater. The over-temp shutdown relay is always activated unless an over-temp is detected. When this occurs, the over-temp relay is deactivated and heating is disabled until the power is removed, the problem is corrected, and power is restored.

4.24 Dual Serial Ports:

On connectors J12 and J14 there are two RS232 serial ports available. The pin-out is compatible with standard format for direct connection to a Personal Computer port using a flat ribbon 10 pin to D style cable that is commonly used in PC's. These ports are capable of 38.4k bits per second. and have full hardware handshake. They are used for communication with other equipment integral to an analysis function such as an FTIR data processor or continuos analyzer.

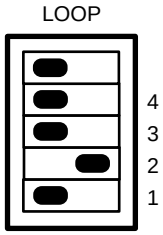
4.25 Expansion I/O connector:

This connector allows access to the Microprocessor bus and other critical signals so that functionality can be added to the ACB2. It is used to connect the Expansion board for LINC, and could be used for other future expansions.

5. Switches

5.1 Setting the loop and Unit switches.

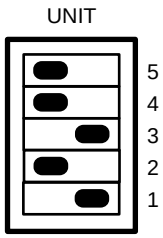
The switches are binary-weighted. The first switch has a value of one or zero, the second switch has a value of two or zero, the third a value of four or zero, the fourth a value of eight or zero, and the fifth a value of sixteen or zero. The values are added and the total is the unit address. The loop switches work the same except only four switches are used for the loop address. The fifth switch is not used. Valid loop numbers are from 1 to 8, and valid unit numbers are from 1 to 31. Setting the loop and unit switches to zero, and cycling power on the unit will clear the current data base. After clearing the data base, set the loop and unit switches to valid settings and cycle the power again.



EXAMPLE: Loop address = 2

BIT = 1,2,4,8, or 16
(OFF)

BIT = 0
(ON)



EXAMPLE: Unit address = 5

6. Setting Jumpers

There are six jumpers on the controller board. All of them should be in the normal position which is shown by a white mark in the silk screen.

Jumper, top view with and without jumper in place.

Jumper Table

Number	Jumper Name	Purpose	Default
JP1	**SPARE INPUT**	**Spare input or ITC detector input**	**ITC input**
JP2	**BAL EN**	**ITC balance enabled or disabled. If using as a spare input, it may be desirable to disable the ITC balance.**	**ITC Balance Enabled**
JP3	**CHART INVERT**	**Chart motor on when output is low or when output is high**	**Active Low**
JP4	**EPROM**	**On-board EPROM can be disabled for test purposes. This jumper should always be enabled**	**Enabled**
JP5	**VRAM**	**The battery backup for the calendar clock and RAM can be disconnected to extend the life of the battery when storing for an extended period.**	**Battery Connected**
JP6	**1M / 4M**	**Option for future expansion to 4 Megabit RAM chips.**	**1 Megabit RAM's**

7. Using the ITC as a Spare Input

If the ITC detector is not needed, its circuitry may be configured as a third spare input. To do this, change Jumper JP1 to the non-default position (see "Setting Jumpers"). If desired, the ITC balance command can be used to balance the output of this spare input, but typically, the balance for a spare input takes place before the signal reaches the ACB. If the signal is balanced before reaching the ACB, the Balance Enable jumper must be moved to the non-default position which will disable the ITC balance.

To connect a spare input:

- **ITC+ is not used.**
- Connect **ITC-** to the signal wire (positive)
- Connect the ground reference signal wire (negative) to the Spare Input GND pin on the ATB (pin 20).

It is unfortunate, but the way the circuitry must be wired puts the positive signal of the spare input on the teminal labeled **ITC-**. This will be a point of confusion, but could not be avoided without creating more confusion somewhere else..

This input must be driven by a low-impedance output. The input impedance is 200 Kohms.

Just as with the other spare inputs, gain is one, and the signal is filtered by a 15 hz low-pass filter before being digitized.

8. Data Table Description

8.1 Overview

The Data Table is a new variable storage area that does not use program table space. It allows users to take advantage of the increased memory of the ACB2 has many similarities to the Result Table.

8.2 Data Table Characteristics:

- Up to 32 independent data tables can be defined which allows one per stream if desired.
- Values can be moved between the Data Table and other tables using Advance Basic.
- Each record contains a value, time, date, and status. Only the value can be written by the user, but all of the fields can be displayed, printed or transferred to other tables.
- The maximum data table size is 65535 records. The minimum data table size is 1.
- The total number of records for all 32 Data Tables is limited by available memory to 73,685.
- One name is associated with all of the records in a Data Table instead of a unique name per record.
- Data Table values are not saved to an Application Cartridge or the APC when the Table Set is saved. Only the table definition which contains the table size and name are saved.
- When a record is written, the status is taken from C(275) in the control table.

8.3 Data Table Record Description

A Data Table Record consists of the following fields. The fields can be read all at once or individually.

Field #	Description	Range
0	Value	Floating Point #
1	Status	0-255
2	Hour	0-23
3	Minute	0-59
4	Second	0-59
5	Month	1-12
6	Day	1-31
7	Year	0-99
8	Name	20 characters (Service Panel display truncates to 17)

8.4 How to work with the Data Table:

8.4.1 Display a Data Table Definition (Name and # of records defined)

From a Service Panel in Application Mode, enter the following sequence:

"Stream" X "Display" Display the stream corresponding to the Data Table of interest; X is 1 to 32

"Alt" "Data" "Display" Displays the name and size of Data Table "X".

8.4.2 Change the size

From a Service Panel in Application mode, Display the Data Table Definition as described above, then:

Move the cursor past the first comma to the size field

<number> **"Enter"** <number> is the number of records

8.4.3 Change the name

From a Service Panel in Application mode, Display the Data Table Definition as described above, then:

Move the cursor past the second comma to the name field

<name> **"Enter"** <name> is the new data table name

Note: The name is unique to its data table, and all records in a data table have the same name.

8.4.4 Display a Record

From a Service Panel in Maintenance Mode, enter the following sequence:

"Stream" X "Display" Display the stream corresponding to the Data Table of interest; X is 1 to 32

"Data" Y "Display" Display record Y; . Y = 1 to 65535

"Display" display the next record

8.4.5 Enter a value.

From a Service Panel in Maintenance mode, Display the Data Table Record as described above, then:

<number> **"Enter"** <number> is the new value

Note: The value in C(275) is written to the status field, and the date and time are written into their corresponding fields of the Data Table Record when the value is written.

8.4.6 Transfer a data table record FIELD in Advance Basic

LET R(K,N) = DT(I,N,J)

K = Result # (1-255)
N = Stream / Table # (1-32)
I = Data Table Record # (1-65535)
J = Data Table Field # (0-7; defaults to 0)
Refer to Data Table Record Description for details of the Data Table fields.

8.4.7 Transfer a data table value in Advance Basic

LET R(2,3) = DT(500,3) moves the value in record #500 of Data Table #3 into Result #2 of Result Table #3

LET C(275) = B(100) B(100) contains the status for the value in B(K).

LET DT(I,N) = B(K)

I = Data Table Record # (1-65535)
N = Table # (1-32)
K = Buffer # (1-255)

Note: When transferring a VALUE, the data table FIELD code is optional, when not specified, the default is 0.

Note: The value in C(275) is written to the status field, and the date and time are written into their corresponding fields of the Data Table Record when the value is written.

8.4.8 Transmit Data Table Records via Advance Data Hiway:

8.4.8.1 APC/Datalogger:

The following statement will transmit a Data Table record (value, status, time, and date) in ASCII format to a previously specified APC/Datalogger file:

PRINT DT(I,N) I = the record # to be transmitted
N = the Data Table #

8.4.8.2 Host Computer:

Each field of a data table record except for the name can be sent to a Host Computer. The following example moves the first 8 fields of Record I from Data Table N to Result Table N beginning with Result #11 and then transmits those results over the Advance Data Hiway in binary format to a Host Computer Interface whose address is loop #1 unit #30.

```
FOR J = 0 TO 7
LET R(11+J,N) = DT(I,N,J)
NEXT J
TRT N,8,11,1,30
```